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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/872,478	06/01/2001	Valerie Jo Young	26152/11:2	9496

3528 7590 06/21/2005

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EXAMINER	
PATEL, JAY P	

ART UNIT	PAPER NUMBER
2666	

DATE MAILED: 06/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/872,478	YOUNG ET AL.	
	Examiner	Art Unit	
	Jay P. Patel	2666	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 January 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-9,11-15 and 19-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *2-9,11-15 and 21-38* is/are allowed.

6)☒ Claim(s) *19 and 20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 January 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 19 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Muhammad et. al (US Patent No. 6650649 B1) further in view of Lozowick et. al (US Patent No. 5307345).

3. In regards to claims 19 and 20, Muhammad teaches A system for interfacing a continuous stream of serial TDM data to a network processor coupled to a parallel data bus. The interface system comprising: an input port for receiving at least one input stream of serial TDM data. Each input data stream comprising a continuous series of time-domain multiplexed time slots synchronized to a common frame pulse signal, each time slot corresponding to a respective virtual channel for carrying digital voice content. This embodiment is anticipated by a quad DS1/AAL1 SSI module (Figure 20 and column 45 lines 55 through 67 continued on column 46 lines 1 through 6). Muhammad discloses a multi-transport cell bus, which is connected to a cell formatter, which extracts the necessary data from the bus (column 46 lines 31 through 35). The cells referred to by the reference are timeslots that carry distinct channels. It is further disclosed that the quad DS1/AAL1 SSI module is a dual transport mode module;

therefore, "it can be configured to work in either TDM mode or ATM AAL1 mode" (column 46 lines 9 through 12). Figure 18 in the reference, discloses a timing diagram for the multi-transport cell bus; therefore it is inherent that the data on the multi-transport cell bus is synchronized to a pulse signal (column 53 lines 10 through 16). It is also inherent from the reference that the disclose invention provides users with " voice, video, and data connections to other networks: (column 2 lines 6 through 9). A receive component coupled to the input port and including a receiver buffer memory for assembling received TDM input data so as to form first bytes of parallel data is anticipated by a receive buffer which copies the data from the cell formatter; furthermore, the receiver buffer is static RAM. It is further disclosed that as the cells are copied, the cell formatter unpacks them in to DSOs as necessary with TDM buffering (column 47 lines 34 through 40). An output port for transmitting at least one output stream of serial TDM data is anticipated by the multi-transport cell bus (column 47 lines 18 through 22). The multi-transport cell bus disclosed in this context by the reference, anticipates the TDM output port. A transmit component coupled to the output port and including a transmit buffer memory for disassembling the second bytes of parallel data so as to form the serial output TDM data is anticipated by the transmit buffer disclosed in the reference (Figure 20). In regards to the parallel bus interface, Muhammad discloses that the cell formatter after further processing sends the data to the PCMIF Logic and through a PCM bus, sends the data to the ATM processor; the timing logic also receives timing information from the multi-transport cell bus via the cell formatter and then sends data to the ATM processor (column 47 lines 45 through 49 and line 52).

ATM cells are also routed from the cell formatter to the ATM processor via the utopia bus (column 47 lines 1 through 6). The ATM processor sends the data to the T1/E1 framers through the combination of the above-mentioned buses. The combination of the above mentioned buses anticipate the parallel bus interface and the ATM processor anticipates the network processor. In regards to the CPU interface, the control interface and the control register, figure 21 in Muhammad discloses a processing unit; the processing unit is connected to the control logic, the cell formatter, and the ATM processor and the processing unit further contains a microprocessor and a message buffer. The control logic disclosed by the reference anticipates a control interface and a control register claimed.

4. In further regards to clam 19, Muhammad fails to teach the limitation of the control register including at least one packet length register. Lozowick et al. (US Patent No. 5307345) teach the above-mentioned limitation in figure 2. Figure 2 shows a block diagram representation of data flow through a bridge device. In figure 2, the client transmit direct memory access (CT DMA 36) includes a packet length register 54. Therefore, it would have been obvious to one skilled in the art at the time the invention was made to combine the interface disclosed by Muhammad with the packet length register disclosed in Lozowick. The proper motivation is supported by Lozowick where reducing latency is a goal "if the packet length is not at the beginning of the received packet there is always going to be an unavoidable latency" (see column 1 lines 52-54).

5. In further regards to claim 20, Muhammad fails to teach the limitation of the CPU interface component including a receive count register and a transmit count register to

allow the network processor to monitor the receive and transmit component buffer memories. Lozowick et. al (US Patent No. 5307345) teaches the above-mentioned limitation. Figure 3 discloses a flowchart of the cut-through operation of a data packet in the bridge system. It is discloses that as each byte or received data is transferred to the buffer memory, the byte counter is incremented. This byte counter is the receive count register since it reflects the number of bytes received from the network (see column 5 lines 50-55). Also evident in figure 3 on the transmit side, at step 76, the packet length is set to maximum after the client transmit direct access memory (CT DMA) resets the byte counter. And at step 78, CT DMA byte counter is incremented for each byte.

Allowable Subject Matter

6. Claims 2-9, 11-15 and 21-38 are allowed.

7. The following is a statement of reasons for the indication of allowable subject matter:

8. With regards to claim 2, the cited references taken individually or in combination fail to particularly disclose **the receive memory is organized so as to define at least tow logical receive memory banks, and each of the receive memory banks is selectively configurable as either an active memory bank available for storing a series of said data bytes as provided by the serial-to-parallel converter, or as a non-active memory bank available for transferring previously stored data bytes to the parallel bus interface.**

It is noted that the closest prior art Muhammad et al. (U. S. Patent 6,650,649 B1) discloses a quad DS1/AAL1 SSI module (Figure 20 and column 45 lines 55 through 67 continued on column 46 lines 1 through 6). Furthermore, Muhammad discloses a multi-transport cell bus, which is connected to a cell formatter, which extracts the necessary data from the bus (column 46 lines 31 through 35). The cells referred to by the reference are timeslots that carry distinct channels. It is further disclosed that the quad DS1/AAL1 SSI module is a dual transport mode module; therefore, "it can be configured to work in either TDM mode or ATM AAL1 mode" (column 46 lines 9 through 12). Figure 18 in the reference, discloses a timing diagram for the multi-transport cell bus. The reference also discloses a receive buffer which copies the data from the cell formatter; furthermore, the receiver buffer is static RAM. It is further disclosed that as the cells are copied, the cell formatter unpacks them in to DSOs as necessary with TDM buffering (column 47 lines 34 through 40). The cell formatter after further processing sends the data to the PCMIF Logic and through a PCM bus, sends the data to the ATM processor; the timing logic also receives timing information from the multi-transport cell bus via the cell formatter and then sends data to the ATM processor (column 47 lines 45 through 49 and line 52). ATM cells are also routed from the cell formatter to the ATM processor via the utopia bus (column 47 lines 1 through 6). The ATM processor sends the data to the T1/E1 framers through the combination of the above-mentioned buses. However, it is noted that Muhammad et. al and the cited references taken individually or in combination, fail to particularly disclose or render obvious the above-mentioned underlined limitations.

9. With regards to claim 11, the cited references taken individually or in combination, fail to particularly disclose **the transmit memory is organized so as to define at least two logical transmit memory banks, each transmit memory bank sized for storing a plurality of said data bytes for serialization into a frame of serial TDM data; each or the transmit memory banks is selectively configurable as either an active memory bank, available for unloading stored data bytes, or as a non-active memory bank available for storing data bytes as they are received from the parallel bus interface.**

It is noted that the closest prior art Muhammad et al. (U. S. Patent 6,650,649 B1) disclose that traffic enters the T1/E1 framers and then data flows to the AALI SAR, which is a part of the ATM processor (column 47 lines 14 through 18). Muhammad also discloses a transmit buffer in figure 20. The data from the transmit buffer flows in to the cell formatter where it is multiplexed onto the multi-transport cell bus (column 47 lines 18 through 22). However, it is noted that Muhammad et. al and the cited references taken individually or in combination, fail to particularly disclose or render obvious the above-mentioned underlined limitations.

10. With regards to clam 21, the cited references taken individually or in combination, fail to particularly disclose **wherein the CPU interface module includes at least one status register for handshaking with the network processor.**

It is noted that the closest prior art Muhammad et al. (U. S. Patent 6,650,649 B1) discloses a quad DS1/AAL1 SSI module (Figure 20 and column 45 lines 55 through 67 continued on column 46 lines 1 through 6). Furthermore, Muhammad discloses a multi-

transport cell bus, which is connected to a cell formatter, which extracts the necessary data from the bus (column 46 lines 31 through 35). The cells referred to by the reference are timeslots that carry distinct channels. It is further disclosed that the quad DS1/AAL1 SSI module is a dual transport mode module; therefore, "it can be configured to work in either TDM mode or ATM AAL1 mode" (column 46 lines 9 through 12). Figure 18 in the reference, discloses a timing diagram for the multi-transport cell bus. The reference also discloses a receive buffer which copies the data from the cell formatter; furthermore, the receiver buffer is static RAM. It is further disclosed that as the cells are copied, the cell formatter unpacks them in to DSOs as necessary with TDM buffering (column 47 lines 34 through 40). The cell formatter after further processing sends the data to the PCMIF Logic and through a PCM bus, sends the data to the ATM processor; the timing logic also receives timing information from the multi-transport cell bus via the cell formatter and then sends data to the ATM processor (column 47 lines 45 through 49 and line 52). ATM cells are also routed from the cell formatter to the ATM processor via the utopia bus (column 47 lines 1 through 6). The ATM processor sends the data to the T1/E1 framers through the combination of the above-mentioned buses. However, it is noted that Muhammad et. al and the cited references taken individually or in combination, fail to particularly disclose or render obvious the above-mentioned underlined limitations.

11. With regards to clam 23, the cited references taken individually or in combination, fail to particularly disclose **the receive component including logic for notifying the network processor when data in the buffer memory is ready for unloading.**

It is noted that the closest prior art Muhammad et al. (U. S. Patent 6,650,649 B1) discloses a quad DS1/AAL1 SSI module (Figure 20 and column 45 lines 55 through 67 continued on column 46 lines 1 through 6). Furthermore, Muhammad discloses a multi-transport cell bus, which is connected to a cell formatter, which extracts the necessary data from the bus (column 46 lines 31 through 35). The cells referred to by the reference are timeslots that carry distinct channels. It is further disclosed that the quad DS1/AAL1 SSI module is a dual transport mode module; therefore, "it can be configured to work in either TDM mode or ATM AAL1 mode" (column 46 lines 9 through 12). Figure 18 in the reference, discloses a timing diagram for the multi-transport cell bus. The reference also discloses a receive buffer which copies the data from the cell formatter; furthermore, the receiver buffer is static RAM. It is further disclosed that as the cells are copied, the cell formatter unpacks them in to DSOs as necessary with TDM buffering (column 47 lines 34 through 40). The cell formatter after further processing sends the data to the PCMIF Logic and through a PCM bus, sends the data to the ATM processor; the timing logic also receives timing information from the multi-transport cell bus via the cell formatter and then sends data to the ATM processor (column 47 lines 45 through 49 and line 52). ATM cells are also routed from the cell formatter to the ATM processor via the utopia bus (column 47 lines 1 through 6). The ATM processor sends the data to the T1/E1 framers through the combination of the above-mentioned buses. However, it is noted that Muhammad et. al and the cited references taken individually or in combination, fail to particularly disclose or render obvious the above-mentioned underlined limitations.

12. With regards to claim 24, the cited references taken individually or in combination fail to particularly disclose **wherein the receive component includes a standby buffer memory and logic for notifying the network processor when data in the buffer memory is ready for unloading; and further includes logic for storing data in the standby buffer memory while data in the buffer memory is unloading to the network processor.**

It is noted that the closest prior art Muhammad et al. (U. S. Patent 6,650,649 B1) discloses a quad DS1/AAL1 SSI module (Figure 20 and column 45 lines 55 through 67 continued on column 46 lines 1 through 6). Furthermore, Muhammad discloses a multi-transport cell bus, which is connected to a cell formatter, which extracts the necessary data from the bus (column 46 lines 31 through 35). The cells referred to by the reference are timeslots that carry distinct channels. It is further disclosed that the quad DS1/AAL1 SSI module is a dual transport mode module; therefore, "it can be configured to work in either TDM mode or ATM AAL1 mode" (column 46 lines 9 through 12). Figure 18 in the reference, discloses a timing diagram for the multi-transport cell bus. The reference also discloses a receive buffer which copies the data from the cell formatter; furthermore, the receiver buffer is static RAM. It is further disclosed that as the cells are copied, the cell formatter unpacks them in to DSOs as necessary with TDM buffering (column 47 lines 34 through 40). The cell formatter after further processing sends the data to the PCMIF Logic and through a PCM bus, sends the data to the ATM processor; the timing logic also receives timing information from the multi-transport cell bus via the cell formatter and then sends data to the ATM processor (column 47 lines

45 through 49 and line 52). ATM cells are also routed from the cell formatter to the ATM processor via the utopia bus (column 47 lines 1 through 6). The ATM processor sends the data to the T1/E1 framers through the combination of the above-mentioned buses. However, it is noted that Muhammad et. al and the cited references taken individually or in combination, fail to particularly disclose or render obvious the above-mentioned underlined limitations.

13. In regards to claim 25, the cited reference fails to disclose **a TDM bridge product with a time slot switch means mounted on the circuit board and coupled to the first input connector for controllably selecting at least one time slot of the TDM input data and providing the selected time slot of serial data to a local bus.**

It is noted that the reference does disclose a cell formatter and a multi-transport cell bus. The reference discloses that the cell formatter listens to the configured timeslot from the multi-transport mode cell bus; however, it fails to disclose the means by which the process takes place and therefore, fails to disclose or render obvious the above underlined limitations as claimed.

14. In regards to claim 31, the cited reference fails to disclose a method for **providing a plurality of N + 1 memory banks, where N is a positive integer; storing a first frame of the series of bytes into a first one of the memory banks; storing each subsequent frame of the series of bytes into a next succeeding one of the memory banks, until N frames of data are stored in respective memory banks; storing a next subsequent frame of the series of bytes in the N+ I th memory bank; and while storing said next subsequent frame of the series of bytes in the**

N+ I th memory bank, concurrently unloading the first N frames of data from the first N memory banks into a processor; responsive to a next frame pulse signal, rotating the memory banks; and then repeating said steps of storing and unloading the series of data bytes in an ongoing fashion for continuous real-time operation; and concurrently, in the processor, encapsulating the wide words of data so as to form a series of data packets bearing the TDM data; and transmitting the series of data packets on to a packet switched network.

It is noted that the reference does disclose receive, transmit and message buffers; however, it fails to disclose the means by which bytes of data are organized in the buffers and furthermore fails to disclose a successive process for loading and unloading bytes of data. Therefore, the reference fails to disclose or render obvious the above underlined limitations as claimed.

Conclusion

15. References not relied upon in the office action but considered pertinent to the art are as follows:

a. US Patent No. 6522648 B1: Parallel backplane architecture providing asymmetric bus time slot cross-connect capability: Heering et. al.

b. US Patent No. 6760333 B1: Hybrid digital subscriber loop and voice-band universal serial bus modem: Moody et. al

c. US Patent No. 6341313: Flow controlling method and apparatus for network between processors: Kanoh, Yasushi

d. US Patent No. 6697383 B1: Method and apparatus for detecting data streams with specific pattern: Li et. al

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jay P. Patel whose telephone number is (571) 272-3086. The examiner can normally be reached on M-F 9:00 am - 5:00 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Seema Rao can be reached on (571) 272-3174. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JPP 6/13/05
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Art Unit 2666

DANG TON
PRIMARY EXAMINER